UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,345	06/28/2001	Krishnamurthy Soumyanath	42390.P11206	8325

7590 11/17/2004

Seth Z. Kalson
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
NGUYEN, HAI L	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,345	SOUMYANATH ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,4,6,9,10,12,22 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,4,6,9,10,12,22 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's appeal brief filed on 8/24/2004 has been received and entered in the case. Applicant's arguments with respect to the prior art rejections mailed on 02/20/2004 have been fully considered and found persuasive, as such; the prior art rejections have been withdrawn. A new action on the merits appears below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3, 4, 9, 10, 22, and 23 are rejected, under 35 U.S.C. 103(a) as being unpatentable over Rogers (US Pat. 5,561,383; previously cited) in view of Asakawa et al. (US Pat. 4,258,310), and further in view of Mehrotra et al. (US Pat. 6,686,300).

With regard to claims 3 and 4, Rogers discloses in Fig. 1b an averaging circuit, and a method of use thereof, comprising an input port (the left one) having an input signal voltage; an output port (the right one) having an output voltage; wherein the output voltage is indicative of a local time-average maximum of the input signal voltage. The reference circuit meets all the claimed limitations except for the element between the input port and the output port is a resistor instead of a field-effect-transistor (502 in instant Fig. 5). Asakawa et al. teaches in Fig. 4c that resistor and field-effect-transistor having gate and source connected together as recited in the

claim, are functionally equivalent. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to replace the resistor in the averaging circuit of Rogers by the field-effect-transistor in order to reduce the size of the circuit because the field-effect-transistor can be fabricated on the chip. Furthermore, Mehrotra et al. teaches in Fig.1 that an increase in leakage current with decreasing gate width is increasing drive current (see column 1, lines 48-60). In other words, the field-effect-transistor has a higher leakage current in term of higher ampere per micron of device width and typically in excess of 1 microampere per micron of device width will have the advantage of increasing drive current. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to increase the leakage current of the field-effect-transistor in the averaging circuit in order to provide stronger drive current for subsequent circuits. Thus, the limitation "wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width" is also met by the references.

With regard to claim 22, the averaging circuit further comprises an output circuit (the capacitor in Fig. 1b of Rogers).

Claims 9, 10, and 23 are similarly rejected; note the above discussion with regard to claims 3, 4, and 22. Since, it is well known in the art for circuit designers to reverse the direction of the field-effect-transistor mentioned above in order to reverse the polarity of the output (see Figs. 1C, 1D, 8C, 8D of Kogan; US Patent 5,321,656; previously cited).

4. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA), Fig. 4 in the present application, in view of Pathak (US Pat. 5,828,603), and further in view of Mehrotra et al.

The APA in Fig. 4 shows a circuit to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising an input port (IN in instant Fig.4) having the input signal voltage; a field-effect-transistor (402); and a DC offset correction unit (406) responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage. Fig. 4 of the prior art meets all the claimed limitations, except that the field-effect-transistor is not configured as recited in the claim. Pathak teaches in Fig. 1 that field-effect-transistor, having gate connected to bias voltage, and a field-effect-transistor, having gate and source connected together as recited in the claim, are functionally equivalent. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to implement the field-effect-transistor in the circuit of APA by using the field-effect-transistor having the gate and source connected together taught by Pathak in order to provide the DC offset correction voltage as a local time-average maximum/minimum of the input signal voltage. Furthermore, the limitation "wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width" is also met by the references; note the above discussion with regard to claims 3 and 4.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
November 5, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800